ДЕГРАДАЦІЯ, МЕТРОЛОГІЯ І СЕРТИФІКАЦІЯ СЕНСОРІВ

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INVESTIGATION OF THE CAUSES OF SILICON MOS — TRANSISTOR PARAMETERS CATASTROPHIC DEGRADATION

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Abstract

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The paper is aimed at finding out the causes of the catastrophic degradation of parameters of silicon MOS-transistors, formed by the ordinary planar technology. The basic causes of degradation have been found to be:

- thermal compression contacts rupture, which can be explained by formation of intermetallic compounds in the contact area, resulting in brittleness of the contacts,
- breaking of the metallic interconnections and contact pads integrity, resulting from inobservance of the photolithography technological conditions as well as from presence of a developed defect structure on the silicon surface and formation of silicide compounds.

Key words: catastrophic degradation, MOS — transistor, silicon. **Анотація**

ДОСЛІДЖЕННЯ ПРИЧИН КАТАСТРОФІЧНОЇ ДЕГРАДАЦІЇ ПАРАМЕТРІВ КРЕМНІЄВИХ МОН — ТРАНЗИСТОРІВ

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Робота присвячена виявленню причин катастрофічної деградації деградації параметрів кремнієвих МОН-транзисторів, які були сформовані за звичайною планарною технологією. Встановлено, що основними причинами деградації є:

- обрив термокомпресійних контактів, який можна пояснити виникненням в районі контакту інтерметалевих з'єднань, що приводить до охрупчування контактів;
- порушення цільності металевої розводки і контактних площин, виникаючих в наслідок порушення технологічних режимів фотолітографії, а також присутності розвиненої дефектної структури на поверхні кремнію і виникнення силіцидних сполук.

Ключові слова: катастрофічна деградація, МОН — транзистор, кремній.

Аннотация

ИССЛЕДОВАНИЕ ПРИЧИН КАТАСТРОФИЧЕСКОЙ ДЕГРАДАЦИИ ПАРАМЕТРОВ КРЕМНИЕВЫХ МОП- ТРАНЗИСТОРОВ

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Работа посвящена выявлению причин катастрофической деградации параметров кремниевых транзисторов, которые были сформированы по обычной планарной технологии. Установлено, что основными причинами деградации являются:

- обрыв термокомпрессионных контактов, которые можно объяснить образованием в районе контакта интерметаллических соединений, приводящих к охрупчиванию контактов;
- нарушение цельности металлической разводки и контактных площадок, возникающие вследствие нарушения технологических режимов фотолитографии, а также присутствия развитой дефектной структуры на поверхности кремния и образования силицидных соединений.

Ключевые слова: катастрофическая деградация, МОП — транзистор, кремний.

Introduction

Variation, instability and catastrophic degradation of silicon MOS-transistor parameters are largely determined by several causes, viz.: by the structural perfection condition of the initial material, and by the condition of their production process.

Effect of structural and point defects in silicon wafer as — delivered, and of those, formed after oxidation and metallization, detected by means of chemical treatments on MOS-transistor parameters are well investigated and described (see, for instance [1,2]).

Complexities of technological processes, consisting of tens of various operations and transitions, imperfections and instabilities of some technological operations, employment of manual work in performing a large number of operations result in deviation from technological parameters and, as a consequence, in appearance of device manufacturing process defects. A quality control system should be implemented in order to detect the defects and to remove the defective structures from the further production cycle as well as to check how the manufactured MOS-transistors meet the technological conditions requirements.

The object and the subject of the research

The object and subject of the research consist in investigation of the causes of catastrophic parameters degradation of encased MOS-transistors, manufactured on p-Si (10(100)) silicon wafers by the usual planar process, and whose parameters have cata-strophically degraded. By "catastrophic degradation", a complete failure of MOS-transistors immediately after manufacture or after a long operation of the devices (over 20000 hours) is understood.

Methods of investigations

Investigation of the causes of catastrophic silicon MOS-transistor parameters degradation was carried out by scanning electron microscopy methods on a "Cam-Scan" scanning electron microscope with a "Link-860" X-Ray microanalyser. The quantitative X-Ray microanalysis was performed using the ZAF-4/F2S program. The MOS-transistor structures underwent argon and chemical layer-by-layer etching [3,4]. The metal was removed in a NaOH alkaline solution, SiO_2 was etched off in hydrofluoric acid followed by washing in deionized water. Argon etching was carried out under the voltage of 1. 5 kV, the beam current being 35 mA; the angle between the sample and the argon beam was 90°, and the etching time was from 25 to 43 minutes. The I-V characteristics were measured in the following modes: the gate voltage U_G=(2-4) V; the drain-source voltage и^=(6-10) V, the drain current I_d=(5-10) mA. From the MOS-transistor lot of 2000 pcs,
those transistors were selected, which failed immediately, and those, which had worked for 20000 hours in the above-mentioned modes before the failure. After that, the transistor cases were carefully opened and investigations were carried out by the above-said methods.

Discussion of the scientific results and conclusions

Figs. 1 (a,b) show the pictures of the disclosed latent defects, breaking of integrity of the metallized path to the gate, and mechanical damage of the pad for thermal compression, which come out after ionic etching for 25 minutes. Survey of this area in the reverse-biased electrons and absorbed current mode has shown that there are sections of lower conduction and break area. A micro-X-Ray spectrum analysis of the current conducting path has revealed the presence of both aluminum and molybdenum, and Al Si and Mo Si silicides in it. Intermetallic com-
x 2 x 2
pounds of Al Au and Al Au Mo types have been found in the area of thermal compression contacts
(Figs. 2).

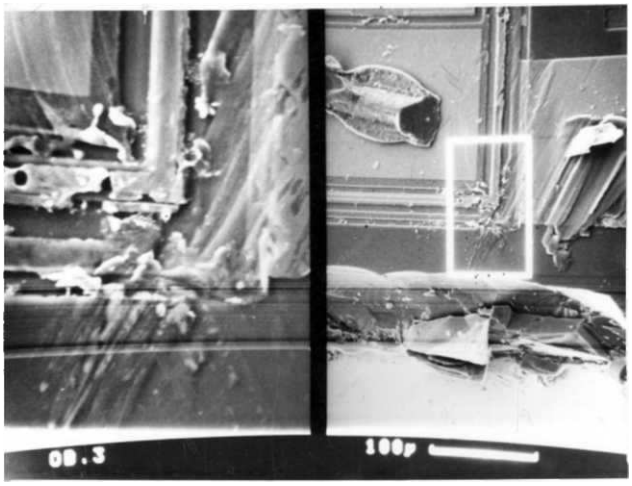

Fig. 1,a Image of the metallization integrity breaking defect.

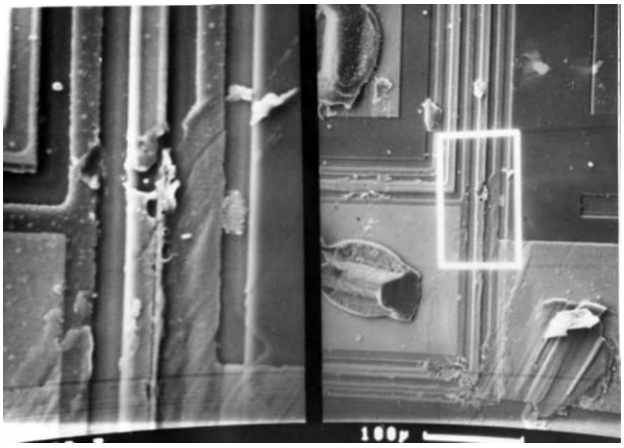

Fig. 1,b. Image of the metallization integrity breaking defect (photolayer etching).

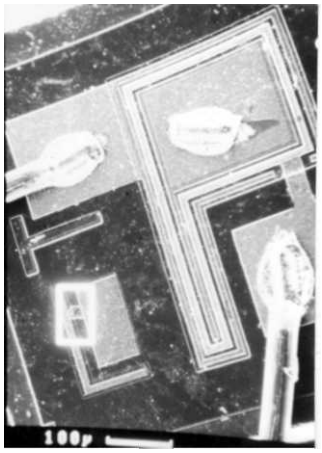

Fig. 2. Image of the thermal compression contact break picture (general view).

Let us consider the basic mechanisms, causing breaks of thermal compression contacts. When connecting the metallized pads on a MOS-transistor with the outer pins of the casing, gold wire is used, which is connected to the source, drain and gate contact pads by way of thermal compression welding.

The revealed intermetallic compounds led to brittleness and, as a consequence, to ruptures of the thermal compression gold-aluminum contacts.

These compounds have a complex composition, depending on the conditions of their formation (gold and aluminum concentrations, temperature and pressure in the thermal compression process, free silicon presence, ambient temperature and service time of the ready MOS-transistor). Due to the difference in the lattice constants, formation of these compounds gives rise to mechanical stresses at the interface. It is well known that the yield point of crystalline substances depends on temperature [5]. The contacts are heated by the current flow, and as a consequence, in destruction of the contact. A detailed analysis of the failure mechanism has made it possible to find out, that interaction and interdiffusion of gold and aluminum occur in the process of thermal compression welding at the temperature of about 300° C, the diffusion rate of gold into aluminum being higher due to the higher value of gold diffusivity (Fig. 3). This diffusion causes formation at the Au-Al interface of intermetallic compounds, whose lattice constants parameters and thermal expansion coefficients differ from the similar lattice parameters of Au and Al, which gives rise to mechanical stresses. Metallization discontinuities have been found to be localized in areas of maximum dislocation clusters (Figs. 4) or lamellar nonuniformity defects clusters (Figs. 5), when the metallization is pickled off and the silicon

surface is treated with Secco (100) or Sirtl (111) [3,4] selective etchant. Despite the good metal-to-silicon adhesion, mechanical stresses arose in these areas, which caused destruction of the metal. Some cases of breaking the metallization uniformity could be associated with metal etching under a photoresist. The experiments have shown the metallization breaking to be largely dependent on the device formation technology.

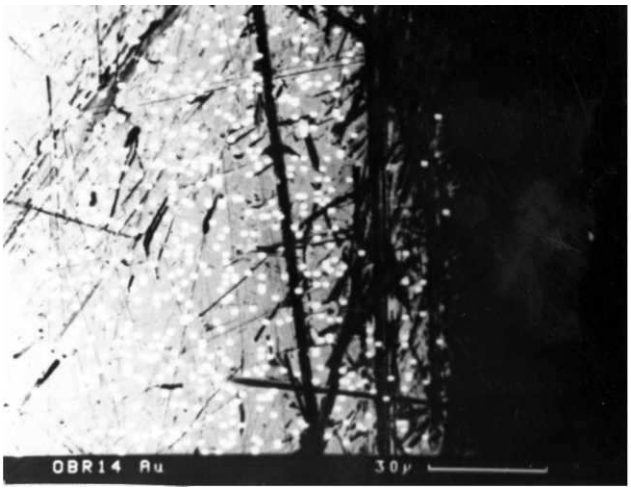

Fig. 3. Electronic image of the gold to aluminum diffusion process.

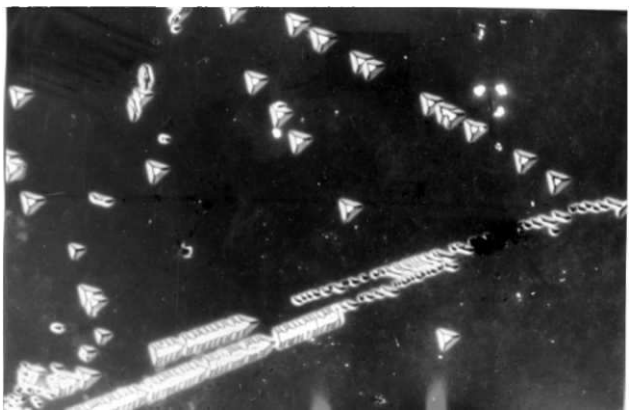

Fig. 4. Electronic image of the dislocation cluster areas, revealed on the silicon surface after removal of the faulty metallization and treatment with the Secco selective etchant.

Particular difficulties arise in the process of photo-lithography. The thickness and quality of the resistive layer are known to be dependent on the photoresist viscosity, manner of its application, temperature and humidity of the ambient, and the substrate surface properties. It has been found out, that the hydrophilic-ity of the substrate surface contributes to etching off the pattern, by facilitating the penetration of the etch-ant under the edge of the photoresist film. The uniformity of the resist layer depends on the metal plating properties. A minutest unevenness in the metal film caused rupture of the photoresistive layer and, as a consequence, etching of metal in the further operations. Besides, it is necessary to strictly maintain the temperature conditions of the photolithography process. Inobservance of the drying conditions led to incomplete removal of the solvent, which caused, in its turn, shielding of the resist's photosensitive properties under exposure. If drying was performed at low temperatures, then poor adhesion of the photolayer to the substrate was observed and cohesion predominated; as a result of it, the photoresist peeled off under development, causing the pattern damage.

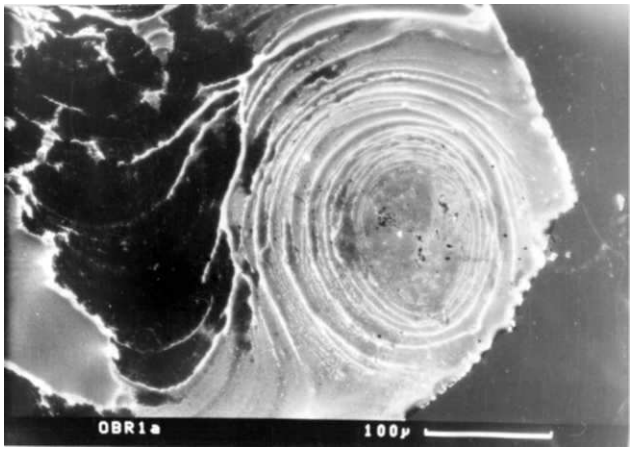

Fig. 5. Electronic image of the lamellar nonuniformity defect, revealed on the silicon surface after removal of the faulty metallization and treatment with the Secco selective etchant.

It has also been found, that even a minor deviation from the norm of at least one of the development process factors (developer concentration, time, temperature, etc.) involved either distortion of the margin edge acutance or a partial photolayer daniage, which subsequently resulted in defects of the current-conducting paths and contact pads.

A large lot of the devices, which had failed after a long operation time, consisted of those ones, whose current-conducting paths and thermal compression contacts hadn't suffered any visible changes. Their detailed analysis has shown, that the catastrophic parameters degradation has occurred because of an abrupt rise of the current, flowing through the gate. An X-Ray analysis of the oxide layers quality has shown the presence of a large amount of metallic impurities in the oxide, their density reaching the maximum value at the silicon-oxide and metal-oxide interfaces (see the Table). It was observed, that the metal impurities density was maximum in more porous oxides. Besides the metal impurities, the X-Ray analysis has

revealed a high concentration of free (uncombined) oxygen in the oxides. It is obvious, that diffusion of impurities towards the metal-oxide and silicon-oxide interfaces took place in the device operation process, causing changes in the potential barriers heights. The probability of tunneling and drain currents rise was increasing due to the presence of a high concentration of states at the oxidesilicon interface[6]. All these factors resulted in an abrupt rise of the current flowing through the gate, and as a consequence, in an abrupt device parameters degradation.

An X- Ray analysis of the oxide layers quality at the oxide-silicon interface

ELMT	% ELMT	ATOM.%
Si	46.064	32,786
Cl	0.201	0.125
Al	0.238	0.221
O	52.633	66.067
Na	0.360	0.300
K	0.520	0.500

Table

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